



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Yasuyuki TAMURA et al.**

Serial No.: **10/765,894**

Group Art Unit: **UNASSIGNED**

Filed: **January 29, 2004**

Examiner: **UNASSIGNED**

For: **SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME**

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 CFR 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 29, 2004

Sir:

Applicants direct the attention of the Patent and Trademark Office to the documents listed on the attached Form PTO-1449. A copy of each listed document is attached.

No fee or certification is required in connection with this Information Disclosure Statement, because it is being submitted prior to the issuance of a first official action on the merits or expiration of the three month period following the filing date or the entry of the national stage of the above-captioned application.

The above information is presented so that the Patent and Trademark Office can, in the first instance, determine any materiality thereof to the claimed invention. Applicants respectfully request that the information be expressly considered during the prosecution of this application and that the documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.



The Commissioner is authorized to charge our Deposit Account No. 50-2866 for any fee that is required to effect consideration of this statement.

Respectfully submitted,

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Enclosures: PTO-1449 and 3 references

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SGA/arf

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U.S. PATENT OFFICE

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	Applicant(s): Yasuyuki TAMURA et al.		
	Filing Date: January 29, 2004		Group Art Unit: Unassigned

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA					
_____	AB					

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Country	Translation (Yes or No)
_____	AC			
_____	AD			

OTHER DOCUMENTS

_____	AE	E.P. Gusev et al., "Ultrathin high-K gate stacks for advanced CMOS devices," International Electron Devices Meeting Technical Digest (2001), pp. 451-454.
_____	AF	W. Zhu et al., "HfO ₂ and HfAlO for CMOS: Thermal Stability and Current Transport," International Electron Devices Meeting Technical Digest (2001), pp. 463-466.
_____	AG	Y. Tamura et al., "Electrical characteristics of SiO ₂ /High-k stacked gate insulator," Extended Abstracts (The 49 th Spring Meeting, 2002); The Japan Society of Applied Physics and Related Societies, No. 2, 28p-A-10, p.820.
Examiner		Date Considered